

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/603,147
Filing Date June 23, 2000
Inventor John T. Moore et al.
Assignee Micron Technology, Inc.
Group Art Unit 2813
Examiner Kielin, Erik J.
Attorney's Docket No. MI22-1443
Title: Capacitor Constructions, DRAM Constructions and Semiconductive
Material Assemblies

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: Jennifer J. Taylor, Ph.D. (Tel. 509-624-4276; Fax 509-838-3424)
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Dear Sir:

The Examiner's attention is directed to the references which are listed on the attached Form PTO-1449 and copies of which are attached.

Citation of these references is respectfully requested.

A check in the amount of \$180.00 is enclosed to cover the fee specified under 37 C.F.R. § 1.17(p).

Respectfully submitted,

Dated:

January 16, 2004

By:

Jennifer J. Taylor
Jennifer J. Taylor, Ph.D.
Reg. No. 48,711

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LIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)APPLICANT
John T. Moore et al.FILING DATE
June 23, 2000GROUP
2813

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
AA		5,976,991	11-1999	Laxman			
AB		6,284,665 B1	09-2001	Lill et al.			
AC							
AD							
AE							
AF							
AG							
AH							
AI							
AJ							
AK							
AL							

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM							
	AN							
	AO							
	AP							
	AQ							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		Stanley Wolf et al., "Silicon Processing for the VLSI Era", 1986, pages 191-195.
	AS		
	AT		

EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.